Patent

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Docket No.8677-US-PA
Application No.: 10/064,767

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Applicant : Li et al.
Application No. : 10/064,767
Filed : Aug. 15, 2002
For : DEVICE AND METHOD FOR MEASURING JITTER IN PHASE LOCKED LOOPS
Art Unit : 2858
Examiner : BENSON, WALTER

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Assistant Commissioner for Patents
Arlington, Virginia 22202

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Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Patent

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Application No.: 10/064,767

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE LI, Sung-Hung et al.

Application for Patent

Filed Aug. 15, 2002

Serial No. 10/064,767

FOR:
DEVICE AND METHOD FOR MEASURING JITTER IN PHASE LOCKED LOOPS

APPEAL BRIEF

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I. REAL PARTY IN INTEREST

The real parties in interest are Sung-Hung LI, Steven SU, Hsin-Chieh LIN, the inventors named in the subject application, and VIA Optical Solution, Inc., the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences.

III STATUS OF THE CLAIMS

A total of 18 claims were presented during prosecution of this application. Claim 4, 5, 14 and 15 are objected but considered to be allowable. Claims 1-3, 6-13 and 16-18 are rejected. Applicants appeal rejected claims 1-3, 6-13 and 16-18.

IV STATUS OF THE AMENDMENTS

Applicants did not file any Amendment on Claims.

V SUMMARY OF THE INVENTION

The present invention is directed to the signal jitter measuring device, which can be also implemented in a PLL, and the measuring method for the jitter.

More specifically, the present invention with respect independent claims 1, 8, and 16, as for example shown in FIG. 4, is to measure the jitter between the input signal S_in and the output signal S_out from the PLL. Wherein, the phase-relationship detection unit 405 can produce ***a phase relationship signal*** (jit-shrt) according to the signals S_in and S_out. In

more detail (page 10, lines 8-14), the phase relation signal, output from the phase-relationship detection unit 405, is to indicate whether or not the output signal is lead or lag.

In addition, the jitter-level output unit 402 is coupled to the phase-relationship detection unit 405 and responsive to the first phase difference signal PDUP, the second phase difference signal PDDN and the phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out) that corresponds to the level of jitter between the output signal and the input signal of the phase locked loop.

Further still, the two phase difference signals PDUP and PDDN are generated as recited in dependent claims 6-7, 9-10, and 17-18, which are described in FIGs. 5 and 6 as the example.

VI ISSUES

A. Were claims 1, 6-7, 8-11 and 16-18 properly rejected under 35 U.S.C. 102(b) as being anticipated by Mesuda et al. (U. S. Patent 5,563,921; hereinafter Mesuda)?

B. Were claims 2-3 and 12-13 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Mesuda in view of Pisipaty (U. S. Patent 6,628,112)?

VII GROUPING OF THE CLAIMS

Applicant proposes three groups of claims to stand or fall together. The first group includes claims 1-3 and 6-7 ("Group I"). The second group includes claims 8-13 ("Group II"). The third group includes claims 16-18 ("Group III").

VIII ARGUMENTS

A. The related law

The standard for lack of novelty (i.e. anticipation) is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements.

Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. ... These elements must be arranged as in the claim under review, ... but this is not an 'ipsissimis verbis' test. *In re Bond*, 910, F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The inquiry as to anticipation is symmetrical with the inquiry as to infringement of a patent. A classic test of anticipation provides: That which will infringe, if later, will anticipate, if earlier. *Knapp v. Morss*, 150 U.S. 221, 37 L. Ed. 1059, 14 S. Ct. 81 (1893); *Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1459, 221 U.S.P.Q. 481 (Fed. Cir. 1984). Therefore, by analogy, the all elements rule used for a determination of infringement finds its applicability in a determination of anticipation. Discussion of the all elements rule can be found in *Becton Dickinson and Co. v. C.R. Bard Inc.*, 17 U.S.P.Q. 2d 1962, 1967 (Fed. Cir 1989) and *Hi-Life Products Inc. v. American National Water-Mattress Corp.*, 6 U.S.P.Q.2d 1132, 1133 (Fed. Cir. 1988).

In addition, a prima facie case of obviousness requires that the reference teachings "appear to have suggested the claimed subject matter." *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143, 147 (CCPA 1976). To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

B. The rejections

Were claims 1, 6-7, 8-11 and 16-18 properly rejected under 35 U.S.C. 102(b) as being anticipated by Mesuda et al. (U. S. Patent 5,563,921; hereinafter Mesuda)?

1. The rejections

As to claims 1, 8 and 16, the Examiner states as follows: Mesuda discloses a signal jitter measuring device for quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal [Fig. 1], the measuring device comprising:

a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between the output signal and the input signal of the phase locked loop (17, Fig. 2; col. 7, lines 11-13 and col. 8, lines 27-33);

a jitter-level output unit coupled to the phase-relationship detection unit and responsive to the first phase difference signal, the second phase difference signal and the phase relationship signal for generating a jitter-level output signal that corresponds to the

level of jitter between the output signal and the input signal of the phase locked loop (17a, 17b, Fig 2; col. 7, lines 13-17 and col. 8, lines 16-26);

where the jitter-level output signal is a pulse width difference between the first phase difference signal and the second phase difference signal (col. 7, lines 25-29.

As to claims 6, 9, and 17, the Examiner states as follows: Mesuda discloses a signal jitter measuring device for quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device comprising:

where the first phase difference signal is asserted at the data transition points of the input signal and de-asserted at the next trigger transition point of the output signal after the generation of the second phase difference signal, and the second phase difference signal is asserted at the next non-triggered transition point of the output signal after the data transition of the input signal, and the second phase difference signal is maintained for a full cycle of the output signal (Fig. 3; col. 7, lines 30-40).

As to claims 7, 10, and 18, the Examiner states as follows: Mesuda discloses a signal jitter measuring device for quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device comprising:

where the first phase difference signal is asserted at the triggering transition points of the input signal when the phase of the input signal leads the output signal and de-asserted at subsequent triggering transition points of the output signal, the second phase difference signal is asserted at the triggering transition points of the output signal when the input signal lags

behind the output signal and de-asserted at subsequent triggering transition points of the input signal (col. 7, lines 20-29).

As to claim 11, the Examiner states as follows: Mesuda discloses a signal jitter measuring device for quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device comprising:

a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between the output signal and the input signal of the phase locked loop (col. 8, lines 14-17); and

a jitter-level output unit coupled to the phase-relationship detection unit and responsive to the first phase difference signal, the second phase difference signal and the phase relationship signal for generating the jitter-level output signal (17, 18, Fig. 1; col. 7, lines 55-59).

2. The prior art

Mesuda (fig. 1; fig. 2; col. 7, lines 11-17; col. 8, lines 27-39; block 17, 18) fails to disclose the features discussed above. The Office Action specifically refers to fig. 2. In fig.2, the two input signals are |f1 – f3| and f2. Then considering the whole circuit as shown in fig. 1 of Mesuda, the frequency converter 14 receives the target signal with the frequency f1 and the reference signal with the frequency f3. The frequency f3 is obtained by f3 = M*f2. Then, the frequency converter 14 produces the signal with frequency of |f1 – f3|. The block 17 receives an output signal having the frequency |f1-f3| from the frequency converter (block 14) and an output signal having the frequency f2 from the voltage-controlled

crystal oscillator (block 11), wherein f3=M * f2. The frequency f2 is feed back signal from the output of frequency converter 17 itself and several other blocks 19, 18, 20, and 11.

In Mesuda, clearly, the block 17 does not receive the input signal S_in and the output signal S_out as recited in claimed invention. The two frequency signal |f1 – f3| and f2 are not the input signal S_in and the output signal S_out of the invention when considering the whole operation.

1. The prior art distinguished

a) Group I

With respect to independent claim 1, the prior art reference Mesuda fails to disclose, show, or suggest all the claim limitations of Group I. Applicants disagree with the Examiner's interpretation of Mesuda.

In Mesuda, clearly, the block 17 does not receive the input signal S_in and the output signal S_out as recited in claimed invention. The two frequency signal |f1 – f3| and f2 are not the input signal S_in and the output signal S_out of the invention when considering the whole operation.

In the present invention, the jitter-level output unit 402 is operated with the phase-relationship detection unit 405 and responsive to the first phase difference signal PDUP, the second phase difference signal PDDN and the phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out) that corresponds to the level of jitter between the output signal and the input signal of the phase locked loop.

The circuit in Fig. 1 of Mesuda clearly fails to disclose the features recited in claim 1 that the jitter-level output unit 402 is coupled to the phase-relationship detection unit 405 and responsive to the first phase difference signal PDUP, the

second phase difference signal PDDN and the phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out).

Therefore, Mesuda fails to disclose all limitations of the claimed invention. Independent claim 1 is not anticipated by Mesuda.

Furthermore, the two phase difference signals PDUP and PDDN are generated as recited in dependent claims 6-7, which are described in FIGs. 5 and 6 as the example.

With at least the same foregoing reasons, dependent claims 6 and 7 are not anticipated by Mesuda either.

b) Group II

With respect to independent claim 8, as with Group I, the prior art reference Mesuda does not disclose, show, or suggest all the limitations of Group II.

Group II is directed to a phase locked loop, using the phase detection circuit and the signal jitter measuring device, including some similar features as discussed above.

Mesuda fails to disclose all limitations of the claimed invention. Independent claim 8 and dependent claims 9 and 10 are not anticipated by Mesuda.

Further with respect to claim 11, the phase-relationship detection unit and the jitter-level output unit of the signal jitter measuring device are further defined. With at least the same foregoing reasons in Group I, Mesuda fails to disclose the phase-relationship detection unit and the jitter-level output unit of the signal jitter measuring device in the same operation.

c) Group III

With respect to independent claim 16, as with Group I, the prior art reference Mesuda does not disclose, show, or suggest all the limitations of Group III.

Group III is directed to a method of measuring signal jitter, which is capable of qualifying the jitters between an input signal and an output signal of a phase looked loop.

Independent claim 16 recites :

> 16. A method of measuring signal jitter which is capable of quantifying the jitters between an input signal and an output signal of a phase locked loop, comprising the steps of:
> *providing a first phase difference signal and a second phase difference signal;*
> *acquiring a phase relationship signal capable of showing whether the phase of the output signal leads or lags the input signal; and*
> *acquiring a jitter value indicating the difference in pulse width between the first phase difference signal and the second phase difference signal according to the phase relationship signal (emphasis added).*

As discussed in Group I, the circuit of Mesuda does not disclose, in operation, the method as recited in independent claim 16.

With respect to dependent claim 17 and 18, the operations of the first phase difference signal and the second phase difference signal are recited. Mesuda either fails to disclose the recited methods.

Were claims 2-3 and 12-13 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Mesuda in view of Pisipaty (U. S. Patent 6,628,112)?

1. The rejections

The Examiner rejected claims 2-3 and 12-13 as being unpatentable over Mesuda in view of Pisipaty. The Examiner applied Mesuda as in the rejection of claims 1 and 8. The Examiner notes that Mesuda fails to disclose all of the features recited in claims 2, 12, 3 and 13. Then, the Examiner cites Pisipaty to disclose a phase detection circuit including:

Where the phase-relationship detection unit comprises:

a triggering unit responsive to the input signal of the phase locked loop for generating a triggering signal [claims 2, 12] (402, 404, Fig. 4, col. 5, lines 10-11);

a D-type flip-flop taking the output signal of the phase locked loop as its input data and the triggering signal as its input clock to produce the phase relationship signal [claims 2, 12] (col. 5, lines 11-17) ***which prevents timing errors***;

where the trigger unit includes:

a delay circuit for delaying the input signal to produce a delayed input signal [claims 3m, 13] (col. 7, lines 15-18);

a XOR gate for receiving the input signal and the delayed input signal and producing the triggering signal [claims 3m, 13] (col. 7, lines 52-54) ***to allow operation at higher frequencies***.

2. The prior art

Pisipaty discloses a PLL circuit 400 in Fig. 4 (col. 5, lines 7-17). Data is fed to the D flip-flop 404 via the node 402, then a clock is output from the VCO 436.

3. The prior art distinguished

a) Group I

The Examiner in above "D-type flip-flop" states that " ...(col. 5, lines 11-17) ***which prevents timing errors*** *(Emphasis added)*". Actually, Pisipaty does not specifically disclose that the design is to prevent timing errors.

The Examiner in above "XOR gate" states that "...(col. 7, lines 52-54) ***to allow operation at higher frequencies*** *(Emphasis added)*". Actually, Pisipaty does not specifically disclose that the design is to allow operation at higher frequencies.

Even though Pisipaty individually uses the D-type flip-flop and the XOR gate, the whole circuit in operation does not supply the missing features in dependent claims 2 and 3, which depend on the parent independent claim 1. The circuit should be considered as a whole for the operation.

Dependent claims 2 and 3 patently define over Mesuda in view of Pisipaty as well.

b) Group II

With at least the same foregoing reasons applied in Group I, dependent claim 12 and 13 patently define over Mesuda in view of Pisipaty as well.

IX CONCLUSION

As noted, none of the cited art, either Mesuda alone or Pisipaty in combination, can be said anticipating or render obvious to the appealed claims.

Accordingly, Applicants believe that the rejections under 35 U.S.C. 102 and 103 are in error, and respectfully request the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully submitted,

Date : August 13, 2004

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APPENDIX A - CLAIMS ON APPEAL

1. A signal jitter measuring device for quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal therein, said measuring device comprising:

a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between said output signal and said input signal of the phase locked loop; and

a jitter-level output unit coupled to said phase-relationship detection unit and responsive to said first phase difference signal, said second phase difference signal and said phase relationship signal for generating a jitter-level output signal that corresponds to the level of jitter between said output signal and said input signal of the phase locked loop;

wherein said jitter-level output signal is a pulse width difference between said first phase difference signal and said second phase difference signal.

2. The signal jitter measuring device of claim 1, wherein the phase-relationship detection unit comprises:

a triggering unit responsive to said input signal of the phase locked loop for generating a triggering signal; and

a D-type flip-flop taking said output signal of the phase locked loop as its input data and said triggering signal as its input clock to produce said phase relationship signal.

3. The signal jitter measuring device of claim 2, wherein the triggering unit includes:

a delay circuit for delaying said input signal to produce a delayed input signal; and

a XOR gate for receiving said input signal and said delayed input signal and producing said triggering signal.

6. The signal jitter measuring device of claim 1, wherein the first phase difference signal is asserted at the data transition points of said input signal and de-asserted at the next trigger transition point of said output signal after the generation of said second phase difference signal, and the second phase difference signal is asserted at the next non-triggered transition point of said output signal after the data transition of said input signal, and the second phase difference signal is maintained for a full cycle of said output signal.

7. The signal jitter measuring device of claim 1, wherein the first phase difference signal is asserted at the triggering transition points of said input signal when the phase of said input signal leads said output signal and de-asserted at subsequent triggering transition points of said output signal, the second phase difference signal is asserted at the triggering transition points of said output signal when said input signal lags behind said output signal and de-asserted at subsequent triggering transition points of said input signal.

8. A phase locked loop having an input signal and an output signal, and capable of providing information on signal jitter, said phase locked loop comprises:

a phase detection circuit in respond to said input signal and said output signal for providing a first phase difference signal and a second phase difference signal; and

a signal jitter measuring device coupled to said phase detection circuit and responsive to said first phase difference signal and said second phase difference signal for generating a jitter-level output signal that corresponds to the jitter level between said input signal and said output signal of said phase locked loop;

wherein said jitter-level output signal is related to the difference in pulse width between said first phase difference signal and said second phase difference signal.

9. The phase locked loop of claim 8, wherein the first phase difference signal is asserted at the data transition points of said input signal and de-asserted at the next triggered

transition points of said output signal after the generation of said second phase difference signal, the second phase difference signal is asserted at the next non-triggered transition points of said output signal after data transition of said input signal, and said second phase difference signal is maintained for a full cycle of said output signal.

10. The phase locked loop of claim 8, wherein said first phase difference signal is asserted at the triggering transition points of said input signal when the phase of said input signal leads said output signal and de-asserted at subsequent triggering transition points of said output signal, and said second phase difference signal is asserted at said triggering transition points of said output signal when said input signal lags behind said output signal and de-asserted at subsequent triggering transition points of said input signal.

11. The phase locked loop of claim 8, wherein the signal jitter measuring device comprises:

a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between said output signal and said input signal of the phase locked loop; and

a jitter-level output unit coupled to said phase-relationship detection unit and responsive to said first phase difference signal, said second phase difference signal and said phase relationship signal for generating said jitter-level output signal.

12. The phase locked loop of claim 11, wherein the phase-relationship detection unit comprises:

a triggering unit responsive to said input signal of said phase locked loop for generating a triggering signal; and

a D-type flip-flop taking said output signal of said phase locked loop as its input data and said triggering signal as its input clock to produce said phase relationship signal.

13. The phase locked loop of claim 12, wherein the triggering unit includes:

a delay circuit for delaying said input signal to produce a delayed input signal; and

a XOR gate for receiving said input signal and said delayed input signal and producing said triggering signal.

16. A method of measuring signal jitter which is capable of quantifying the jitters between an input signal and an output signal of a phase locked loop, comprising the steps of:

providing a first phase difference signal and a second phase difference signal;

acquiring a phase relationship signal capable of showing whether the phase of said output signal leads or lags said input signal; and

acquiring a jitter value indicating the difference in pulse width between said first phase difference signal and said second phase difference signal according to said phase relationship signal.

17. The method of claim 16, wherein the first phase difference signal is asserted at the data transition points of said input signal and de-asserted at the next triggering transition points of said output signal after the generation of said second phase difference signal, and the second phase difference signal is asserted at the next non-triggered transition points of said output signal after data transition of said input signal and the second phase difference signal is maintained for a full cycle of said output signal.

18. The method of claim 16, wherein the first phase difference signal is asserted at the triggering transition points of said input signal when the phase of said input signal leads said output signal and de-asserted at subsequent triggering transition points of said output signal, and the second phase difference signal is asserted at the triggering transition points of said

output signal when said input signal lags behind said output signal and de-asserted at subsequent triggering transition points of said input signal.